

## U.S. Patent Application

### **MICRODISPLAY PACKAGING SYSTEM**

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## MICRODISPLAY PACKAGING SYSTEM

### BACKGROUND

A microdisplay integrated circuit (IC) includes a two-dimensional array of pixel cells formed on a semiconductor substrate. Each pixel cell may be adapted to control an electric field across an associated portion of liquid crystal material. The electric field may be modulated to change a state of the liquid crystal material in order to produce an image pixel of a desired pixel intensity for a given image frame. Current microdisplay IC packages attempt to protect microdisplay IC components and to provide an environment for proper operation thereof.

### 10 BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic side cross-sectional view of a microdisplay IC according to some embodiments.

FIG. 2 is a plan view of a microdisplay IC package according to some embodiments.

FIG. 3A is an exploded view of a microdisplay IC package according to some  
15 . . . . . embodiments.

FIG. 3B is an exploded view of a microdisplay IC package according to some  
embodiments.

FIG. 4 is a plan view of a microdisplay IC package according to some embodiments.

FIG. 5A is an exploded view of a microdisplay IC package according to some  
20 . . . . . embodiments.

FIG. 5B is an exploded view of a microdisplay IC package according to some  
embodiments.

FIG. 6 is a plan view of a microdisplay IC package according to some embodiments.

FIG. 7 is a plan view of a microdisplay IC according to some embodiments.

FIG. 8 is an exploded view of a microdisplay IC package according to some embodiments.

FIG. 9 is a plan view of a microdisplay IC package according to some embodiments.

FIG. 10 is a flow diagram of a process according to some embodiments.

5 FIG. 11 is a top view of a wafer including a plurality of microdisplay ICs.

FIG. 12 is side view of a wafer and a base prior to coupling according to some embodiments.

FIG. 13 is side view of a wafer and a base after coupling according to some embodiments.

10 FIG. 14 is side view of a wafer and a base prior to coupling according to some embodiments.

FIG. 15 is a block diagram of an image display system according to some embodiments.

## DETAILED DESCRIPTION

15 FIG. 1 is a schematic side cross-sectional view of a portion of microdisplay IC 10 according to some embodiments. Microdisplay IC 10 is a Liquid Crystal on Silicon (LCoS) device, but embodiments are not limited thereto. Rather, embodiments may be implemented with Liquid Crystal Diode (LCD) devices, Digital Micromirror Display (DMD) devices, or devices using any other suitable microdisplay technology.

20 Microdisplay IC 10 includes semiconductor substrate 15. Substrate 15 may comprise single-crystal silicon or any other semiconductor substrate within which integrated electrical devices may be fabricated. In this regard, pixel cell array 20 is fabricated within the upper layers of semiconductor substrate 15. Pixel cell array 20 may be fabricated using currently- or hereafter-known masking, etching, and deposition techniques.

FIG. 1 shows three pixel cells 21 within pixel cell array 20. Pixel cells 21 may be arranged in a two-dimensional grid of equally-spaced pixel cells. In some embodiments the two-dimensional grid may include thousands of pixel cells 21 on a side. Each pixel cell 21 of the grid may correspond to a single image pixel of microdisplay IC 10.

5        Each pixel cell 21 is associated with a pixel electrode 22. Pixel electrode 22 may comprise a reflective material such as aluminum for reflecting light incident thereto. One pixel electrode 22 may be used to selectively apply a voltage signal, or potential, to a region of light switching layer 25 with which it is in contact. In this regard, light switching layer 25 may comprise a layer of liquid crystal of any suitable type.

10        According to some embodiments, pixel electrodes 22 comprise an array of micromirrors, and light switching layer 35 may comprise air. Pixel electrodes 22 themselves may operate to switch light in such embodiments.

      Electrode 30 may contact light switching layer 25 to complete an electric circuit to carry current through a voltage source (not shown), pixel cell 21, pixel electrodes 22, light  
15        switching layer 25, electrode 30, and back to the voltage source. In some embodiments, electrode 30 comprises Indium Tin Oxide.

      As shown in FIG. 1, electrode 30 is disposed between light switching layer 25 and substantially transparent protective cover 35. Cover 35 may comprise glass coated with an anti-reflective material to increase a percentage of incident light that passes through cover  
20        35 and on to switching layer 25.

      For purposes of the present description, microdisplay 10 will be described as including elements 15 through 30. Additionally, elements 20 through 30 will be generally referred to as imaging elements. A microdisplay IC according to some embodiments may comprise less or more imaging elements than shown in FIG. 1.

25        In operation, a pixel cell 21 of pixel cell array 20 generates a voltage on an associated pixel electrode 22. The voltage is applied to a region of light switching layer 25 that is in contact with the associated pixel electrode 22. The applied voltage may, in conjunction with a voltage signal applied to electrode 30, create an electric field across the

region of light switching layer 25. More specifically, a strength of the electric field is based on a potential difference between the applied potential and a potential of electrode 30. The region of light switching layer 25 reacts to the electric field according to its characteristic behavior.

5           In this regard, each region of light switching layer 25 may operate as an electrically-activated light filter. When subjected to a weak or no electric field, a region may impart no polarization rotation to light that is received through cover 35, thereby preventing the light from passing to the reflective surface of a pixel electrode 22 that is in contact with the region. When subjected to a stronger electric field, the region may rotate light received  
10 through cover 35 forty-five degrees as it passes through the region of light switching layer 25. The light then reflects off the reflective surface of the pixel electrode 22 and is rotated an additional forty-five degrees as it passes back through the region before exiting cover 35. A percentage of incoming light that is reflected back through cover 35 can therefore be varied by varying the strength of the electric field.

15           According to some embodiments, each region of light switching layer 25 controls an intensity of light returned through cover 35 based on the strength of an applied electric field. Some embodiments of light switching layer 25 direct light received through cover 35 using other techniques.

          To form an image using microdisplay IC 10, a desired intensity is determined for  
20 each pixel of the image. Electric field intensities that correspond to the desired image pixel intensities are then applied to regions of light switching layer 25 that correspond to the image pixels. As a result, any light that is incident to cover 35 will reflect off of pixel electrodes 22 and exit from cover 35 toward an observer in accordance with the desired pixel intensities. Microdisplay IC 10 may display a moving image by rapidly displaying  
25 successive images. In such a case, the successive images may be referred to as image frames.

          The intensities of pixels displayed by microdisplay IC 10 therefore depend in part upon the strength of the electric fields applied across corresponding regions of light

switching layer 25. The strength of these fields depends in part on a distance between electrode 30 and pixel electrodes 22 that are in contact with the corresponding regions. This distance may be specified by the design of microdisplay IC 10. In a case that this distance is outside of designed tolerances for one or more pixels, pixel intensities displayed by  
5 microdisplay IC 10 may not correspond to desired pixel intensities.

The distance between one or more of pixel electrodes 22 and electrode 30 may fall outside of the designed tolerances if microdisplay IC is mechanically distorted. For example, some conventional systems bond the substrate of a microdisplay IC directly to a substantial chip carrier. The chip carrier may possess a coefficient of thermal expansion  
10 (CTE) that differs significantly from the CTE of the microdisplay IC. Heat generated by the microdisplay IC during operation may cause the chip carrier to expand at a different rate than the microdisplay IC, thereby causing mechanical distortion of the microdisplay IC.

FIG. 2 is a plan view of a microdisplay IC package according to some embodiments. Package 40 includes microdisplay IC 10 and base 50. Base 50 may comprise a material  
15 having a CTE that substantially matches the CTE of cover 35. The material may be substantially identical to the material of cover 35. Moreover, a thickness of base 50 may substantially match a thickness of cover 35. In some embodiments, base 50 may reduce a mechanical distortion of microdisplay IC 10 by increasing a stiffness of microdisplay IC 10. Moreover, base 50 may increase mechanical isolation between microdisplay IC 10 and a  
20 chip carrier to which package 40 may be mounted.

Bonding agent 60 may couple microdisplay IC 10 to base 50. Bonding agent 50 may comprise one or more of thermal epoxy, thermal tape, thermal grease, thermal phase change material, and any other suitable bonding agent. Bonding agent 60 may be applied to one or both of a lower surface of substrate 15 and an upper surface of base 50 to couple  
25 microdisplay IC 10 to base 50.

FIG. 3A is an exploded view of microdisplay IC packaging according to some embodiments. Packaging 70 includes cover 35 and microdisplay IC 10, base 50, chip carrier

80, bonding agent 90, and heat sink 100. Packaging 70 may provide efficient heat dissipation and mechanical isolation of microdisplay IC 10 during operation thereof.

As described with respect to FIG. 2, base 50 may be coupled to microdisplay IC 10 using any suitable bonding agent. Base 50 may be coupled chip carrier 80 using any  
5 suitable bonding agent, including but not limited to thermal epoxy, thermal tape, and thermal grease.

Chip carrier 80 may comprise ceramic and/or organic material. A material of chip carrier 80 may possess a CTE similar to that of semiconductor substrate 15. In some embodiments, the CTE of base 50 matches the CTE of semiconductor substrate 15 more  
10 closely than the CTE of chip carrier 80 matches the CTE of semiconductor substrate 15. Chip carrier 80 defines recess 82. Foot 84 bounds a bottom of recess 82. Foot 84 and chip carrier 80 may be composed of identical or different materials.

Recess 82 is adapted to receive packaging 40. Packaging 40 may mount within recess 82 via any bonding agent mentioned herein. In some embodiments, packaging 40,  
15 and more particularly base 50, is coupled to foot 84. The material of carrier 80 may provide a low thermal resistance path for cooling packaging 40 during operation. The material may also be yielding so as to absorb mechanical deflections of packaging 40. According to some embodiments, foot 84 is substantially less thick than packaging 40 and therefore the stiffness of packaging 40 dominates the stiffness of foot 84 when subjected to mechanically distorting  
20 forces.

Chip carrier 80 also includes conducting pads 86 for transmitting electrical signals to the imaging elements of microdisplay IC 10. Conducting pads 86 may be soldered onto chip carrier 80 and may also be fabricated thereon. In some embodiments, wire bonds couple conducting pads 86 to the imaging elements of microdisplay IC 10.

25 Control chip 88 may include driving elements for driving the imaging elements of microdisplay IC 10. Control chip 88 may also include an interface to an external source for receiving pixel image data from the source. The interface may also be used to receive and

transmit signals used to synchronize the operation of microdisplay IC 10 with other elements of a display system.

Bonding agent 90 is depicted as thermal tape but may comprise any other agent for coupling heat sink 100 to chip carrier 80. Bonding agent 90 may contact at least a portion of foot 84 and heat sink 100. In such a case, a high thermal conductivity path may be established between microdisplay IC 10 and heat sink 100. Moreover, bonding agent 90 may provide mechanical isolation of microdisplay 10 from any differential expansion of heat sink 100.

FIG. 3B is an exploded view of packaging 110 according to some embodiments. Packaging 110 may be identical to packaging 70 except for the exclusion of base 50. Accordingly, a lower surface of semiconductor substrate 15 is coupled directly to foot 84, perhaps with only a bonding agent therebetween. Such embodiments may provide more efficient heat dissipation than embodiments such as packaging 70.

FIG. 4 is an outward view of packaging 70 and/or packaging 110 according to some embodiments. Protective cover 35 is shown protruding from recess 82 of chip carrier 80. In some embodiments, protective cover 35 is substantially flush with an upper surface of chip carrier 80, while in other embodiments cover 35 is recessed beneath the upper surface of chip carrier 80. Cover 35 may completely protrude from recess 82, with an upper surface of microdisplay IC 10 being flush with or extending above the upper surface of chip carrier 80.

FIG. 5A is an exploded view of packaging 120 according to some embodiments. Elements of packaging 120 correspond to similarly-numbered elements described above.

Packaging 120 includes chip carrier 130, which in turn defines opening 135. Other elements of chip carrier 120 except may be identical to elements of chip carrier 80. Packaging 40 may be mounted within opening 135 via friction, a bonding agent, and/or mechanical elements (not shown). Bonding agent 90 may be coupled directly to base 50 and to heat sink 100, thereby possibly providing more efficient heat dissipation than some embodiments such as packaging 70.



FIG. 5B is an exploded view of packaging 140 according to some embodiments. Packaging 140 may consist of elements similar to those of packaging 120, excepting base 50. Therefore, a lower surface of semiconductor substrate 15 is coupled directly to heat sink 100 by bonding agent 90.

5           FIG. 6 is an outward view of packaging 120 and/or packaging 140 according to some embodiments. Protective cover 35 is shown substantially flush with an upper surface of chip carrier 130. In some embodiments, protective cover 35 protrudes from opening 135 of chip carrier 130, while in other embodiments cover 35 is recessed beneath the upper surface of chip carrier 130. As described with respect to FIG. 4, cover 35 may completely protrude  
10   from opening 135, with an upper surface of microdisplay IC 10 being flush with or extending above the upper surface of chip carrier 130.

FIG. 7 is an outward view of a microdisplay IC according to some embodiments. Microdisplay IC 200 comprises substantially transparent protective cover 210 coupled to semiconductor substrate 220. Imaging elements may be fabricated on semiconductor  
15   substrate 220 such that an upper surface of electrode 30 is flush with an upper surface of substrate 220. Other physical arrangements may also be utilized, such as the arrangement of FIG. 1.

At least a portion of the upper surface of semiconductor substrate 220 comprises bonding surface 230. As will be described in more detail, bonding surface 230 may be  
20   coupled to an associated portion of a chip carrier. Bonding surface 230 may be coated with a material suitable for bonding microdisplay IC 200 to a chip carrier. Bonding surface 230 comprises conductors 240 to carry electrical signals to the imaging elements of microdisplay IC 200. Bonding surface 230 and conductors 240 may be fabricated onto substrate 220 using currently- or hereafter-known fabrication techniques.

25           FIG. 8 is an exploded view of packaging 250 according to some embodiments. Packaging 250 comprises microdisplay IC 200, chip carrier 260, bonding agent 270 and heat sink 280.

Chip carrier 260 defines opening 262. Microdisplay IC 200 may be coupled to carrier 260 such that cover 210 extends into opening 262. Chip carrier 260 may include a lip surrounding opening 262 to receive cover 210. Bonding surface 230 may contact surface 264 of carrier 260 and be coupled thereto by a bonding agent. Conductors 240 may contact  
5 associated conductors on surface 264 to allow electrical signals to travel from chip carrier 260 to imaging elements of microdisplay IC 200. Finally, bonding agent 270 may couple heat sink 280 to substrate 220.

FIG. 9 shows packaging 250 according to some embodiments. Cover 210 is shown extending into opening 262. According to some embodiments, cover 210 extends partially  
10 into opening 262. In other embodiments, cover 210 extends fully into opening 262 and an upper surface of cover 210 is flush with surface 266 of carrier 260. Cover 210 may alternatively extend partially through or fully through opening 262.

FIG. 10 is a flow diagram of process 300 according to some embodiments. Process 300 may be executed by manufacturing equipment and/or manually. In this regard, process  
15 300 may be embodied in program code that is executable by manufacturing equipment. The program code may be received from any medium, including but not limited to a hard disk, an IC-based memory, a signal, and a network connection.

Initially, at 301, at least one set of imaging elements is fabricated on an upper surface of a semiconductor substrate. FIG. 11 is a top view of semiconductor wafer 310 on which  
20 sixty sets of imaging elements were fabricated according to 301. Each set of imaging elements may correspond to a single microdisplay IC, and each microdisplay IC includes a semiconductor substrate that is part of wafer 310. Wafer 310 may comprise any semiconductor substrate on which circuit elements may be fabricated, and portions of wafer 310 may be integrated within the imaging elements.

25 A lower surface of wafer 310 is ground at 302 to reduce its thickness. In some embodiments, grinding yields a thin and relatively pliable wafer that may be 0.1mm or less in thickness. The grinding may also allow wafer 310, which may not be flat and which may

include residual mechanical stresses resulting from the fabrication process, to conform to a flat base.

5 A base is affixed to a lower surface of semiconductor wafer 310 at 303. FIG. 12 is a side view of wafer 310 and base 320 after 302 and prior to 303. Base 320 may comprise a material having a CTE that substantially matches the CTE of a substantially transparent protective cover to be coupled to the upper surface of wafer 310. The material may be substantially identical to the material of the protective cover, and/or may have a thickness substantially equal to a thickness of the cover. According to some embodiments, the cover may be coupled to wafer 310 prior to 303.

10 Base 320 may be affixed to wafer 310 so as to generate substantially negligible mechanical stress therebetween when the imaging elements are operated within a range of operating temperatures. According to some embodiments of this aspect, an epoxy is applied to one of base 320 and lower surface 315 of wafer 310. Base 320 and surface 315 are brought into contact with one another while at a temperature equal to at least one operating  
15 temperature of the imaging elements of wafer 310. When at such a temperature, wafer 310 and base 320 may expand (or contract) according to their respective CTEs. The epoxy is then cured at at least one operating temperature of the imaging elements. The curing may be a partial curing, with a final curing subsequently occurring at a higher temperature.

20 Process 300 may thereby result in unit 350 of FIG. 13. Unit 350 may appear as shown when at the at least one operating temperature. Moreover, the sixty individual sub-units that may be formed by dicing unit 350 may each be substantially flat and free of mechanical stresses when at the at least one operating temperature. Such flatness may provide a uniform distance between pixel electrodes 22 and electrode 30 of each sub-unit at the operating temperature.

25 Due to their different CTEs, the interface of wafer 310 and base 320 may be subjected to significant mechanical stresses at other temperatures. These stresses may cause the unit comprised of wafer 310 and base 320, and the individual sub-units to warp into a substantially non-flat shape.

According to other embodiments of 303, base 320 is affixed to wafer 310 to substantially flatten wafer 310. FIG. 15 illustrates wafer 360 that is similar to wafer 310 except for being warped due to various factors. Wafer 360 may be affixed to base 320 by applying a bonding agent therebetween and by pressing base 320 and wafer 360 together  
5 with enough force to substantially flatten wafer 360 and affix the flattened wafer to base 320. A protective cover may be coupled to an upper surface of wafer 360 after process 300.

The previously-described embodiments of 303 may be combined with the present embodiment. Particularly, wafer 360 may be affixed to base 320 while at a temperature equal to at least one operating temperature of the imaging elements of wafer 360. Such a  
10 combination may reduce an amount of mechanical stress at an interface of wafer 360 and base 320 during operation of the imaging elements.

The unit resulting from process 300 may be diced into individual sub-units comprising a microdisplay IC coupled to a portion of base 320. These units may be more mechanically rigid than prior microdisplay IC packages. Moreover, each portion of base  
15 320 may be configured to include a flex cable interface and electrical connections for delivering signals from flex cable to the imaging elements of an associated microdisplay IC.

FIG. 15 is a block diagram of a display system according to some embodiments. Display system 400 may be used to project a color image using one or more microdisplay package(s) 70. Display system 400 comprises light source 402, lens 404, optics 406, and  
20 projector lens 408. Image data source 410 may comprise any device such as a personal computer, a television tuner, a personal digital assistant, and a digital videodisc player. Image data source 410 provides microdisplay package(s) 70 with image data for display.

Light source 402 provides light to display system 400. Light source 402 may comprise a 100W – 500W lamp such as a metal halide lamp or an Ultra High Pressure  
25 (UHP) arc lamp. The light is received by lens 404, which transmits a uniform beam of light to optics 406. Optics 406 may include a dichroic filter for removing non-visible light from the beam of light. Optics 406 may also include one or more mirrors, color filters, and prisms for directing selected spectral bands of light to microdisplay package(s) 70.

Generally, optics 406 may project separate spectral bands of light (e.g., red, green, or blue light) to microdisplay package(s) 70. In some embodiments using three microdisplay packages 70, pixel imaging elements 25 of each microdisplay package 70 are set to imaging states that correspond to pixel intensities of red, green, or blue components of an image.

- 5 Optics 406 project a corresponding spectral band onto each microdisplay package 70, receive reflected light that represents each of the three components of the image from the microdisplay packages 70, combine the reflected light into a single full-color image, and transmit the image to projector lens 408.

- 10 Projector lens 408 receives the transmitted image, which may measure less than an inch across. Projector lens 408 may magnify, focus, and project the image toward a projection screen (not shown). Display system 400 may be located on a same side of the projector screen as the intended audience (front projection), or the screen may be located between the audience and display system 400 (rear projection).

- The several embodiments described herein are solely for the purpose of illustration.
- 15 Embodiments may include any currently or hereafter-known versions of the elements described herein. Therefore, persons skilled in the art will recognize from this description that other embodiments may be practiced with various modifications and alterations.